SYNOPSYS®

新思科技股份有限公司



Job Title	Job Description	Qualification	Location
Application	Provides technical	Typically requires a	HsinChu City
Engineer	support to customers and	BS/MS degree in	
A	internal Synopsy <mark>s teams</mark>	Electronics/Computer	W.
	to solve comple <mark>x</mark>	Engineering with some	W
100	technical issues faced	related work experience	IB ²
Ž.	during the testing of	in IC design industry.	8
	ASICs in leading edge	Working knowledge of	y
100	technologies.	RTL design, synthesis	
A STATE OF THE STA	 Responds to situations to 	and good understanding	
100	isolate or fix problems or	of ASIC design flow.	
	suggest appropriate	Familiar with Synopsys	· .
	workarounds to meet	synthesis, STA, formal	
	critical de <mark>sign schedules.</mark>	verification, P&R and	
	 Provides feedback about 	DFT tools is a plus.	
4	the to <mark>ols and</mark>	V	Shringer Service
Á.	met <mark>hodologies</mark> to product	War.	
	dev <mark>elopme</mark> nt teams to		
	enh <mark>ance</mark> the quality of		
	Syn <mark>op</mark> sys' solutions.		
1	 Involve in project 	And the same	
V	deployment, customer	A	
V	training and on-site	A	<i>y</i>
	support.	ft.	V
DFT Sr. RD	 Working in a project- 	BE+5 years of relevant	HsinChu City
Solution	oriented environment to	experience in Electrical	J.
Engineer	deliver DFT Solutions	Engineering or	
	ranging from defining,	Computer Engineering	
	automating & integration	or other relevant field of	
	of test products to	study	
	supporting Bring-Up on	Experience with	

	Customer designs.	Scan/MBIST
	 Interacting with the 	Diagnostics & Silicon
	customers to assess their	Bring up
	methodologies and flows,	
		Expertise in handling silican debug yield
	gather requirements and	silicon debug, yield
	propose solutions.	ramping, yield
	The primary focus area	management
	(but not limited to) for the	Good understanding of
	DFT Solutions Engineer	ATPG, MBIST, 1500,
	would be SLM (Silicon	1687, LBIST
A	Life Cycle Mana <mark>gement)</mark>	Excellent
<u> </u>	Products.	communication and
A 1	V.	presentations skills.
ASIC Digital	Development of leading	Master degree in EE or HsinChu City
Design	edge DesignWare	CS related engineering
Engineer	processor IP products	● Up to 4 years of
1	such as NN accelerators,	experience in digital
	vision processors, as well	design or verification
	as high-performance or	● Microprocessor
	energy-effici <mark>ent general</mark>	architecture knowledge
	purpose processors.	● HDL and Verification
9	The responsibility could	languages: Verilog
	vary f <mark>rom archit</mark> ecture	Micro-architecture and
A	anal <mark>ysis, micr</mark> o-	RTL design, or
	arc <mark>hitectur</mark> e, logic design	UVM/OVM, functional
	and implementation,	formal & coverage
	formal verification,	Programming skills:
	simulation verification,	SystemVerilog, C/C++,
\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	related engineering flows	plus Python, shell
V.	and environments,	scripts, or assembly
No.	methodology	Tools for RTL linting,
	development, quality	simulation, and
	improvement, product	synthesis
	delivery, as well as SoC	Analytical skills
	implementation and	3.1.2.1
	system bring-up.	
APR 實體設計	Assisting customers tape	● Familiar with Floorplan, HsinChu City/
工程師	out from Netlist to GDS	Place and route, Chupei City
-1-/1土口り	out from Nethal to GDS	r lace and route, Chuper City

- by using Synopsys EDA tools.
- Focus in the areas of design planning, floorplanning, place and route, parasitic extraction, signal integrity analysis and prevention, IR drop/EM analysis and physical verification (DRC/LVS).
- A secondary focus will be in static timing analysis and formal verification.
- Interacts regularly with customers to identify and eliminate barriers to project success.
- Plans and manages delivery of own projectrelated tasks.
- Provides feedback to R&D/AE on suggested tool enhancements or issues.

- DRC/LVS, IR drop, EM and Signal Integrity etc.
- Familiar with STA, Verification and Synthesis.
- Demonstrate physical design implementation experience.
- Demonstrate English communication and customer interfacing skills.
- Travel up to 30%, and put in long hours when required to meet customer deadline on specialized technical or business issues.

企業簡介

新思科技名列美國標普 500 指數成分股,長期以來是全球排名第一的 IC 電子設計自動化(EDA)創新公司,也是排名第一的 IC 介面 IP 供應廠商,專門提供「矽晶到軟體(Silicon to $Software^{TM}$)」最佳的解決方案。不論是針對開發先進半導體系統單晶片(SoC)的設計工程師,或正在撰寫應用程式且要求高品質及安全性的軟體開發工程師,新思科技都能提供所需的解決方案,以協助工程師完成創新、高品質並兼具安全性的產品。更多詳情請造

訪: http://www.synopsys.com。

新思科技 1991 年在台灣成立分公司,並於 2012 年底合併思源科技,目前員工總人數已近千位,其中有超過 500 位的研發人才,是在台灣的跨國軟體企業中,擁有最大規模研發團隊的公司之一。新思科技持續為台灣培養半導體設計軟體人才,加速國內廠商產品開發與問市的時程,強化台灣在半導體國際市場的競爭力。 本公司注重性別工作平等及致力於員工組成多元化,並歡迎符合資格之身心障礙求職者就職。本公司將會依身心障礙求職者之需求、職位及本公司之商業資源,提供適當之無障礙設施。本公司所有有關聘僱、調職、晉升、訓練、工資報酬及績效評估等事項,均會依法及員工個別之表現公平處理之。

福利制度

除法定福利以外,所有正式員工可享有以下公司贊助之福利:

- ◎保險福利:公司全額負擔勞保、健保、團保
- ◎福利活動:福委會社團活動、旅遊補助、生日/三節禮金、婚喪喜慶及生育補助、定期健康檢查
- ○教育訓練制度:鼓勵不斷的學習及自我成長,創造活潑的學習環境,配合個人的長短期生涯規劃,提供完善的教育訓練制度,包括內訓及外訓,技術性及非技術性訓練
- ◎員工購股(ESPP)
- ◎優於勞基法之特休假及部分全薪之事病假
- ◎享每月各項現金津貼